REMARKS

Claims 1-47 are pending in the application.

Claims 2, 5, 12-23, 31, 32, 35, 39, 41, and 43-46 (originally claim 45) are withdrawn as non-elected and are hereby cancelled without prejudice for presentation in a divisional application.

Claims 1, 3, 4, 6-11, 24-30, 33, 34, 36-38, 40, 42 and 47 (originally claim 46) are rejected.

Claims 10, 33, 36, and 47 are amended. In particular, claims 10, 36 and 47 are amended to correct typographical errors in the claim numbers.

New claims 48-51 are added.

No new matter is added.

The Examiner has stated that the title of the invention is not descriptive. The title of the invention is amended hereby as shown above on page 2 of this Amendment.

Claims 1, 3, 4, 6-11, 24-30, 33, 34, 36-38, 40, 42 and 46-51 remain in the case.

Applicant requests reconsideration and allowance of the claims in light of the above amendments and following remarks.

Claim Rejections-35 U.S.C. § 112

Claims 33, 36-38, 40 and 42 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The rejections are respectfully traversed.

The Examiner has stated that it is unclear and confusing to what is meant by "wherein the first bond pad is disposed under the second chip" in claim 33.

Claim 33 is amended to clarify that the first bond pad disposed at an edge of the first chip is also disposed to be under the second chip to further clarify the patentable subject matter of the claimed invention.

In claim 36, the Examiner has stated that "The multi-chip package" lacks antecedent basis. Claim 36 is amended to correct a typographical error, i.e., replacing "the" with "A."

Applicant respectfully submits that the amendment to claim 36 makes claims 37-38, 40 and 42 definite.

Accordingly, claims 33, 36-38, 40 and 42 are now allowable under 35 U.S.C. § 112, second paragraph.

Claim Rejections-35 U.S.C. § 103(a)

Claims 1, 3, 4, 6, 8-11, 24-30, 33, 34, 36-38, 40, 42 and 47 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,503,776 B2 Pai et al., ("Pai") in view of U.S. Patent No. 5,365,091 Yamagishi ("Yamagishi").

Claim 6 is rejected under 35 U.S.C. § 103 (a) as being unpatentable over Pai, in view of Yamagishi, and further in view of U.S. Patent No. 6,239,366 B1 Hsuan et al., ("Hsuan").

The rejections are respectfully traversed.

The claimed invention recited in claim 1 is directed to a multi-chip package including a semiconductor chip structure formed using a re-routing technology. See, for example, FIGS. 8-11 of the present application. In this embodiment, a bond pad-wiring pattern 12, which is an equivalent to a conventional center-type bond pad, is located in a substantially center region of the substrate 11. A passivation layer 16 covers the bond pad wiring pattern 12. In the prior art, the bond pad wiring pattern 12 is normally exposed to form a bond pad, to which bonding wire is attached. However, in the claimed invention, it is instead coupled to a pad-rearrangement pattern 15 for rerouting. A portion of the pad-rearrangement pattern 15 is then exposed to form bond pads 17. See page 6, lines 10-12 and FIG. 8 of the present application. With this rerouting using the pad-rearrangement pattern 15, because the center pad-type chip can be modified into a peripheral pad-type chip, it is possible to vertically stack the multiple chips. See page 11, lines 16-18 of the present application.

Also, according to another aspect of the present invention, the bond pads 17 of this embodiment are formed over at least a part of the cell regions of the substrate 11. See page 6, lines 10-24 of the present application, which states, for example, "the pad-rearrangement pattern 15 reroutes the bond pads 17 from the bond pad-wiring pattern 12 in the peripheral circuit region A_{peri} to above the cell regions A_{cell1} and A_{cell2}." Therefore, the peripheral circuit region A_{peri} has a much smaller width than that of the conventional peripheral circuit region. Thus, the total width of the semiconductor chip 10 can be reduced. Thus, much smaller semiconductor chip can be manufactured compared to the prior art. See page 6, lines 30-34 of the present application.

In contrast, however, Yamagishi has nothing to do with such a rerouting technology and the cited references nowhere teach or suggest the above recited features or advantages of the claimed invention recited in claim 1. In particular, FIGS. 1 and 3 of Yamagishi illustrate that the wiring elements including 9b of Yamagishi are formed substantially at the edge regions of the substrate and nowhere discloses a pad-rearrangement pattern for rerouting the

bond pads from substantially the center region to another region (e.g., an edge) of the chip, as in the claimed invention. Looking specifically at cited FIGS. 1 and 23 of Yamagishi, element 9b, which is indicated by the Examiner as a bond pad wiring pattern, but actually a power leading line, is located close to the edge of the chip 1 and not in a substantially center region. That is, the power leading line 9b is located towards the edge of the chip 1 outside of the peripheral power supply line 8b, particularly between the peripheral power supply line 8b and the bonding pads 7. Thus, Yamagishi does not teach or disclose, "the bond pad-wiring pattern [being] formed substantially in a center region of the semiconductor substrate," as recited in claim 1.

Additionally, the element 25a, 24 indicated the Examiner as a pad rearrangement pattern including bond pads 7 are also *all* located in the peripheral circuit region 3. More particularly, FIGS. 1 and 23 of Yamagishi, and the teachings of Yamagishi at col. 7, lines 7-15 illustrate the positional relationships between the internal circuit region 2 and other wiring elements such as the peripheral power supply lines 8a and 8b, elements 25a, 24, 9b, and the bonding pads 7. Yamagishi therefore teaches the elements 25a, 24, 9b and bond pads 7 are located outside the internal circuit region 2 in the peripheral circuit region 3. Compare these teachings of Yamagishi with, for example, FIG. 11 of the present application.

Further, at column 6, lines 15-18, Yamagishi disclose that the internal circuit region 2 is arranged at the center of the chip 1. And at column 6, lines 31-35, Yamagishi states that "an internal circuit region 2 is surrounded by a peripheral circuit region 3."

In view of the above and because "this internal circuit region 2 is arranged with a plurality of basic cells," as argued by the Examiner, Yamagishi does not teach or disclose that "the pad rearrangement pattern is disposed over at least a part of the cell region," as recited in claim 1.

For these reasons, Yamagishi does not teach or disclose, among other things, "the bond pad-wiring pattern [being] formed substantially in a center region of the semiconductor substrate," "a pad-rearrangement pattern electrically connected to the bond pad-wiring pattern, the pad-rearrangement pattern including bond pads disposed over at least a part of the cell region," as recited in claim 1. Therefore, the cited references, either alone or in combination, fail to disclose each and every element of independent claim 1.

The other independent claims of the present application (claims 24, 36 and 47) all contain an element regarding the bond pad-wiring being formed substantially in a center region of a substrate or chip. At least for the above reasons, the cited references do not teach or disclose, "a bond pad-wiring pattern formed substantially in a center region of the first

chip; and a pad-rearrangement pattern electrically connected to the bond pad-wiring pattern, wherein the pad-rearrangement pattern includes a first bond pad disposed at an edge of the first chip," recited in claim 24 or similarly 36.

In addition, with respect to claim 47, at least for the reasons discussed above, the cited references do not teach or disclose, "bond pad-wiring patterns formed substantially in a center region of the first chip; and pad-rearrangement patterns electrically connected to the bond pad-wiring patterns, wherein the pad-rearrangement patterns include bond pads disposed along opposing edges of the first chip, wherein the spacer is placed between the bond pads."

Thus, these independent claims are believed to be allowable and the applicant respectfully requests their allowance.

Claims 3, 4, 6-10, and 48, which all depend from independent claim 1, are believed to be allowable for their dependency and their own merits. For example, none of the cited references teach or disclose, "a portion of the pad rearrangement pattern extends substantially from the center region of the semiconductor substrate toward an edge of the semiconductor substrate." Accordingly, the applicant respectfully requests their allowance.

Claims 25-30, 33 and 34 all depend from independent claim 24 and for at least the same reasons given for claim 24, these claims are believed to be allowable and the applicant respectfully requests their allowance.

Claims 37, 38, 40 and 42 all depend from independent claim 36 and for at least the same reasons given for claim 36, these claims are believed to be allowable and the applicant respectfully requests their allowance.

With respect to new claims 48-51, all of the claims are allowable for the reasons stated above. For example, with respect to claim 48, none of the cited references teach or disclose, "the spacer is disposed over the bond pad-wiring patterns formed substantially in a center region of the first chip," as recited in claim 48.

For the foregoing reasons, reconsideration and allowance of claims 1, 3, 4, 6-11, 24-30, 33, 34, 36-38, 40, 42 and 47-51 of the application as amended is solicited. The Examiner

is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

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Respectfully submitted,

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Limited Recognition Under 37 CFR § 10.9(b)

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